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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/925,905	08/09/2001	Atsushi Kamashita	1113-016/MMM	6489

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EXAMINER	
BROCK II, PAUL E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/925,905	KAMASHITA ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-24 and 40-55* is/are pending in the application.

4a) Of the above claim(s) *47-55* is/are withdrawn from consideration.

5)☒ Claim(s) *40-46* is/are allowed.

6)☒ Claim(s) *18-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/177254.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 18 – 21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furumiya (USPAT 5637893, Furumiya) in view of the applicant's admitted prior art (AAPA).

With regard to claim 18, Furumiya discloses in figure 1b a method of transferring a charge from a charge accumulation layer to a transistor of a solid picture element so as to substantially eliminate residual images. It should be noted that the limitation "so as to substantially eliminate residual images" is an intended use limitation that does not bear any patentable weight in this method claim. Furumiya discloses in figure 1b locating a charge accumulation region (13) of a first conductive type (n) within a semiconductor substrate having a first surface such that no portion of the charge accumulation region contacts the first surface of the semiconductor substrate. Locating a depletion prevention region (17) within the semiconductor substrate between the charge accumulation region and the first surface. Locating a transfer gate (25) on the first surface of the semiconductor substrate such that the transfer gate overlaps a portion of the charge accumulation region. It is not clear if Furumiya discloses locating a transistor within the semiconductor substrate, the transistor being in communication

with the transfer gate for receiving a charge from the charge accumulation region and amplifying the charge. The AAPA teaches in figure 14 and page 2, lines 7 – 12 locating a transistor (205 – 209) within a semiconductor substrate (201), the transistor being in communication with a transfer gate (210) for receiving a charge from a charge accumulation region (203) and amplifying the charge. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the transistor of the AAPA in the method of Furumiya in order to amplify the photelectrically converted charge and therefore increase the sensitivity of the imaging device as stated by the AAPA on page 1, lines 15 – 25 and page 2, lines 1 – 2.

With regard to claim 19, Furumiya discloses in figure 1b further comprising the step of locating the charge accumulation region so as to orient a first margin of the charge accumulation region toward a far edge of the gate and locating the depletion prevention region so that no portion of the depletion prevention region is closer to the far edge of the gate than the first margin of the charge accumulation region. It would have been further obvious in the method of Furumiya and the AAPA that this relationship with the far edge of the gate would also be true for the transistor.

With regard to claim 20, Furumiya discloses in figure 1b further comprising the step of locating a first margin of the charge accumulation region 0.0 microns closer to the far edge of the gate than any portion of the depletion prevention region. It would have been further obvious in the method of Furumiya and the AAPA that this relationship with the far edge of the gate would also be true for the transistor.

With regard to claim 21, the AAPA teaches on page 2, line 1 wherein the transistor is a field effect transistor.

With regard to claim 24, Furumiya discloses in figures 1b wherein the transfer gate is a metal-oxide semiconductor gate.

3. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furumiya and the AAPA as applied to claim 18 above, and further in view of Gross (USPAT 5734293).

The AAPA teach that the transistor is a JFET type. Furumiya and the AAPA do not teach wherein the transistor is a bipolar transistor or a metal-oxide semiconductor transistor. Gross teaches in column 8, lines 39 – 46 wherein an amplifying transistor is a JFET type or a bipolar transistor or a metal-oxide semiconductor transistor. It would have been obvious to one of ordinary skill in the art to use the bipolar of metal-oxide semiconductor transistor of Gross as a substitute for the JFET of Furumiya and the AAPA in order to maintain the condition that an input bias of a voltage feedback smaller than an input bias of a current feedback amplifier as stated by Gross in column 8, lines 39 – 46. This gives one of ordinary skill in the art the ability to choose transistors based on the technology employed on other areas of the integrated device while not adding additional process steps.

Allowable Subject Matter

4. Claims 40 – 46 are allowed.

Response to Arguments

5. Applicant's arguments filed September 14, 2004 have been fully considered but they are not persuasive.

6. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Therefore, applicant's arguments are not persuasive and the rejection is proper.

7. With regard to applicant's argument that "the cited combination of Furumiya and applicants' prior art improperly picks and chooses features from the cited art without considering the references as a whole," it should be noted that by considering the references as a whole, one of ordinary skill would be motivated to make the suggested combination. Applicant argues that the read-out region 26A of Furumiya would lead away from the subject matter of claim 18 and toward the structure of applicants' prior art Fig. 14. Such an argument is confusing. The rejection of claim 18 uses applicant's prior art figure 14 in combination with Furumiya to make obvious claim 18 (see rejection above). Figure 14 of applicant's prior art clearly teaches that

amplification by use of the transistor (205-209) is useful in an imaging device. Furumiya's layer 26a does not amplify and therefore does not have the same benefits as applicant's admitted transistor. Amplification leads to increased sensitivity of an image device (see AAPA page 1, lines 15 – 25). Thus, one of ordinary skill would recognize that in order gain increased sensitivity in a signal from the imaging device of Furumiya it would have been obvious to use the amplifying transistor of the applicants' admitted prior art in the image pickup device of Furumiya. Therefore, applicant's arguments are not persuasive and the rejection is proper.

8. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Thus, because "no part of Furumiya teaches or suggests a CCD image sensor that includes an amplifying transistor" one of ordinary skill would not be dissuaded to improve sensitivity in Furumiya's image sensor by incorporating an amplifying transistor. Therefore, applicants' arguments are not persuasive and the rejection is proper.

9. With regard to applicants' argument that "the references as a whole would lead one skilled in the art away from the combination proposed byu the examiner," it should be noted that nowhere in the cited prior art is the explicit teaching against the combination. Nowhere in Furumiya is it suggested that an improvement in the sensitivity of the image pickup devices would not be desired. Thus, one can only conclude that increasing the sensitivity of the image

pickup device of Furumiya would be a persuasive reason to use the amplification transistor of the applicant's admitted prior art. Therefore, applicants' arguments are not persuasive and the rejection is proper.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-1723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II